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what will happen if there is setup time  
and hold time violation how to overcome  
this Set up time is the amount of time  
before the clock edge that the input  
signal needs to be stable to guarantee it  
is accepted properly on the clock edge'

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**organized and manipulated When**  
**dealing with data structure we not**  
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**flip flops particularly if the reset is**  
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input But in such a case the combinational logic gate count grows so the overall gate count savings may not be that significant'

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**VGS It  $V_t$  no channel is induced and**

**the MOSFET will be in cut off region**

**No current flows Triode region When**

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**and current starts flowing if VDS gt**

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**The Inputs In Sensitivity Disk If Yes**

**Why Answer Yes in a pure**

**combinational circuit is it necessary**

**to mention all the inputs in**

**sensitivity disk other wise it will**

**result in pre and post synthesis**

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